All approved, except: pages 7, 8, 14, 17 as marked.
3/23/05 JFH

Amendments to the Specification:

Please replace the paragraph bridging pages 10 and 11 with the following amended paragraph:

Ripple reset glitches where simultaneously setting and/or resetting a set of scan cells causes the circuit to go through intermediate states that generate indeterministic reset glitches on other scan cells are solved by using multiple SR_EN signals to break the ripple reset cycle. Since the SR_EN signals of the present invention can either be generated internally or applied externally this does not result in any additional requirement regarding the number of external pins needed for scan-test. Furthermore since scan enable is used to disable the set/reset ports during the shift operation this solution can easily <u>be</u> adapted for either scan-test or self-test, hence overcoming all the shortcomings of prior-art solution #4. The present invention covers the mentioned asynchronous set/reset DFT design-rule violation repair at RTL, gate-level or any other level of abstraction during the design process.

Please replace the paragraph bridging pages 15 and 16 (page 15, line 14 through page 16, line 15) with the following amended paragraph:

Once all asynchronous set/reset violations in a scan-based integrated circuit are repaired, test pattern generation and/or fault simulation is performed on the repaired circuit in order to

improve the fault coverage for set/reset as well as data faults. This method comprises the following computer-implemented steps:

(4-1) Compile the HDL (hardware description language) code modeled at RTL (register-transfer level) or gate-level that represents the ~~repaird~~ repaired scan-based integrated circuit into a sequential circuit model.

(4-2) Specify input constraints on clocks, the set/reset enable (SR_EN) signal, and the scan enable (SE) signal of the ~~repaird~~ repaired scan-based integrated circuit.

(4-3) Transform the sequential circuit model into an equivalent combinational circuit model.

(4-4) Generate and/or fault simulate test patterns according to the specified input constraints and the combinational circuit model.

Please replace the first full paragraph on page 28 with the following amended paragraph:

FIG. 2E shows the result 280 of applying the prior-art #4 solution to repair the asynchronous reset violation shown in FIG. 2A. This solution uses a multiplexor 281 controlled by the external set/reset enable (ESR_EN) signal 282 to disable the asynchronous reset port 284 of the scan cell 205 during scan-test. During the shift operation, the ESR_EN signal 282 is set to logic value 1 so that any data being shifted into the scan cell 205 will not be destroyed. During the capture operation, two options are possible.

In one option, the ESR_EN signal 282 is set to logic value 0 to allow faults in the set/reset circuitry 203 to be detected. In the other option, the ESR_EN signal 282 is set to logic value 1 to disable the asynchronous reset port of the scan cell 205 while the clock CK 209 is applied to test faults propagated from functional logic 204 to the data port 211 of the scan cell 205. In addition, being able to disable the asynchronous reset port of the scan cell 205 also helps to prevent any glitch at the output 210 of the set/reset circuitry 203 from affecting the state of the scan cell 205.

Please replace the paragraph bridging pages 33 and 34 with the following amended paragraph:

FIG. 3C shows an embodiment 370 of a set/reset controller, in accordance with the present invention. The capture controller 376 consists of one inverter 378. The shift controller 377 consists of one NOR gate 379 and one AND gate 380. During the shift operation, the scan enable signal SE 382 is set to logic value 1. As a result, the shift controller 375 will set the asynchronous reset signal 392 of the scan cell 381 to logic value 0. That is, the reset capability of the scan cell 381 will be disabled, preventing the data shifted to this scan cell from being destroyed. After the shift operation is completed, the circuit enters the capture operation when the scan enable signal SE 382 is set to logic value 0. At the first stage of the capture operation, the SR_EN signal

383 is set to logic value 0. As a result, the asynchronous reset signal 392 will remain disabled. The capture clock CK 388 is applied to capture the faults present in the functional logic block 372 into the scan cell 381 via its data input port 389. At the second stage of the capture operation, the capture clock CK 388 is disabled and the SR_EN signal 383 is set to logic value 1. This will set the signal 390 to logic value 1 enabling the propagation of the faults present in the original set/reset circuitry 371 to the scan cell 381 via its asynchronous reset port RESET 392. The numerals 384, 385, 386, 373 and 374 designate the normal input signals to the set/reset circuitry and numeral 387 the output thereof.

Beginning on page 34, first full paragraph and ending with the last paragraph on page 41, please replace the paragraphs with the following amended paragraphs on pages 31 - 41:

FIG. 4A shows a timing diagram 400a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping single-capture clocks. In one test pattern, 4012, 4023 and 4032 designate the shift-in operation, capture operation and shift-out operation, respectively. During the first cycle in the capture operation 402a, two single pulses are applied to the capture clocks CK1 322 and CK2 324 in a non-overlapping manner as shown at 405a and 406a to detect data faults while the global set/reset enable

global_SR_EN 311 is set to logic value 0. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second cycle in the same capture operation 402a, the global set/reset enable global_SR_EN 311 is set to logic value 1 as shown at 404a while the capture clocks CK1 322 and CK2 324 are inactive; as a result, set/reset faults are detected.

FIG. 4B shows a timing diagram 410a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with overlapping single-capture clocks. In one test pattern, 4112, 4122 and 4132 designate the shift-in operation, capture operation and shift-out operation, respectively. During the first cycle in the capture operation 412a, two single pulses are applied to the capture clocks CK1 322 and CK2 324 in an overlapping manner as shown at 415a and 416a to detect data faults while the global set/reset enable global_SR_EN 311 is set to logic value 0. This overlapping capture clock scheme can be used when there is no interaction between two clock domains or clock skews between two clock domains are properly managed. Then, during the second cycle in the same capture operation 412a, the global set/reset enable global_SR_EN 311 is set to logic value 1 as shown at 414a while the capture clocks CK1 322 and CK2 324 are inactive; as a result, set/reset faults are detected.

FIG. 4C shows a timing diagram 420a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping at-speed double-capture clocks. In one test pattern, 421a, 422a and 423a designate shift-in operation, capture operation and shift-out operation, respectively. During the first cycle in the capture operation 422a, two at-speed double pulses are applied to the capture clocks CK1 322 and CK2 324 in a non-overlapping manner as shown at 425a to 428a to detect data faults while the global set/reset enable global_SR_EN 311 is set to logic value 0. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second cycle in the same capture operation 422a, the global set/reset enable global_SR_EN 311 is set to logic value 1 as shown at 424a while the capture clocks CK1 322 and CK2 324 are inactive; as a result, set/reset faults are detected. This timing diagram shows that delay faults in functional logic can be tested with a double-capture approach, in accordance with the present invention. Note that delay faults can also be tested with a single-capture or last-shift-launch approach, in accordance with the present invention.

FIG. 4D shows a timing diagram 430a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the

present invention, where both data faults and set/reset faults are detected during the same capture operation with overlapping at-speed double-capture clocks. In one test pattern, 431a, 432a and 433a designate shift-in operation, capture operation and shift-out operation, respectively. During the first cycle in the capture operation 432a, two at-speed double pulses are applied to the capture clocks CK1 322 and CK2 324 in an overlapping manner as shown at 435a to 438a to detect data faults while the global set/reset enable global_SR_EN 311 is set to logic value 0. This overlapping capture clock scheme can be used when there is no interaction between two clock domains or clock skews between two clock domains are properly managed. Then, during the second cycle in the same capture operation 432a, the global set/reset enable global_SR_EN 311 is set to logic value 1 as shown at 434a while the capture clocks CK1 322 and CK2 324 are inactive; as a result, set/reset faults are detected. This timing diagram shows that delay faults in functional logic can be tested with a double-capture approach, in accordance with the present invention. Note that delay faults can also be tested with a single-capture or last-shift-launch approach, in accordance with the present invention.

FIG. 4E shows a timing diagram 440a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping single-

capture clocks. For test pattern i, 441a, 442a and 443a designate the shift-in operation, capture operation and shift-out operation, respectively, and for test pattern j, 444a, 445a and 446a designate the shift in operation, capture operation and shift-out operation, respectively. During the first capture operation 442a for test pattern i, two single pulses are applied to the capture clocks CK1 322 and CK2 324 as shown at 448a and 449a while the global set/reset enable global_SR_EN 311 is set to logic value 0 for the whole capture operation, in order for test pattern i to detect data faults. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second capture operation 445a for test pattern j, the global set/reset enable global_SR_EN 311 is set to logic value 1 as shown at 447a while the capture clocks CK1 322 and CK2 324 are kept inactive for the whole capture operation, in order for test pattern j to detect set/reset faults.

FIG. 4F shows a timing diagram 450a for testing the design without any ripple structure shown in FIG. 3A, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping at-speed double-capture clocks. In FIG. 4F, for test pattern i, 451a, 452a and 453a designate shift-in operation, capture operation and shift-out operation, respectively; and for test pattern j 454a, 455a and 456a designate the shift-in operation, capture operation

and shift-out operation, respectively. During the first capture operation 452a for test pattern i, two at-speed double pulses are applied to the capture clocks CK1 322 and CK2 324 as shown at 458a to 461a while the global set/reset enable global_SR_EN 311 is set to logic value 0 for the whole capture operation, in order for test pattern i to detect data faults. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second capture operation 455a for test pattern j, the global set/reset enable global_SR_EN 311 is set to logic value 1 as shown at 457a while the capture clocks CK1 322 and CK2 324 are kept inactive for the whole capture operation, in order for test pattern j to detect set/reset faults. This timing diagram shows that delay faults in functional logic can be tested with a double-capture approach, in accordance with the present invention. Note that delay faults can also be tested with a single-capture or last-shift-launch approach, in accordance with the present invention.

FIG. 4G shows a timing diagram 400b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping single-capture clocks. In FIG. 4G, 401b, 402b and 403b designate the shift-in operation, capture operation and shift-out operation, respectively. During the first cycle in the capture operation

402b, three single pulses are applied to the capture clocks CK1 362, CK2 364, and CK3 366 in a non-overlapping manner as shown at 406b to 408b to detect data faults while the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 0. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second cycle in the same capture operation, the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 1 in a non-overlapping manner as shown at 404b and 405b while the capture clocks CK1 362, CK2 364, and CK3 366 are inactive; as a result, set/reset faults are detected. Note that the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are not active at the same time. As a result, any glitch caused by state changes due to the active global set/reset enable signal global_SR_EN1 347 will not affect all scan cells controlled by the global set/reset enable signal global_SR_EN2 346.

FIG. 4H shows a timing diagram 410b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where both data faults and set/reset faults are detected during the same capture operation with non-overlapping at-speed double-capture clocks. In FIG. 4H, 411b, 412b and 413c designate the shift-in operation, capture operation and shift-out operation, respectively. During the first cycle in the capture operation 412b, three at-speed double pulses are applied to the

capture clocks CK1 362, CK2 364, and CK3 366 in a non-overlapping manner as shown at 416b to 421b to detect data faults while the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 0. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second cycle in the same capture operation, the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 1 in a non-overlapping manner as shown at 414b and 415b while the capture clocks CK1 362, CK2 364, and CK3 366 are inactive, as a result, set/reset faults are detected. Note that the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are not active at the same time. As a result, any glitch caused by state changes due to the active global set/reset enable signal global_SR_EN1 347 will not affect all scan cells controlled by the global set/reset enable signal global_SR_EN2 346. This timing diagram shows that delay faults in functional logic can be tested with a double-capture approach, in accordance with the present invention. Note that delay faults can also be tested with a single-capture or last-shift-launch approach, in accordance with the present invention.

FIG. 4I shows a timing diagram 430b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping single-

capture clocks. In FIG. 4I, the test pattern i, 431b, 432b and 433b designate shift-in operation, capture operation and shift-out operation, respectively; and for test pattern j, 434b 435b and 436b designate shift-in operation, capture operation and shift-out operation, respectively. During the first capture operation 432b for test pattern i, three single pulses are applied to the capture clocks CK1 362, CK2 364, and CK3 366 as shown at 439b to 441b while the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 0 for the whole capture operation, in order for test pattern i to detect data faults. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second capture operation 435b for test pattern j, the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 1 as shown at 437b and 438b in a non-overlapping manner while the capture clocks CK1 362, CK2 364, and CK3 366 are kept inactive for the whole capture operation, in order for test pattern j to detect set/reset faults. Note that the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are not active at the same time. As a result, any glitch caused by state changes due to the active global set/reset enable signal global_SR_EN1 347 will not affect all scan cells controlled by the global set/reset enable signal global_SR_EN2 346.

FIG. 4J shows a timing diagram 450b for testing the design with a two-stage ripple structure shown in FIG. 3B, in accordance with the present invention, where data faults and set/reset faults are detected during two capture operations with non-overlapping at-speed double-capture clocks. In FIG. 4J for test pattern i, 451b, 452b and 453b designate shift-in operation, capture operation and shift-out operation, respectively; and for test pattern j, 454b, 455b and 456b designate shift-in operation, capture operation and shift-out operation, respectively. During the first capture operation 452b for test pattern i, three at-speed double pulses are applied to the capture clocks CK1 362, CK2 364, and CK3 366 as shown at 459b to 464b while the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 0 for the whole capture operation, in order for test pattern i to detect data faults. This non-overlapping capture clock scheme is used to avoid the impact of clock skews between two clock domains. Then, during the second capture operation 455b for test pattern j, the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are set to logic value 1 as shown at 457b and 458b while the capture clocks CK1 362, CK2 364, and CK3 366 are kept inactive for the whole capture operation, in order for test pattern j to detect set/reset faults. Note that the global set/reset enable signals global_SR_EN1 347 and global_SR_EN2 346 are not active at the same time. As a result, any glitch caused by state changes due to the active global set/reset enable signal

global_SR_EN1 347 will not affect all scan cells controlled by the global set/reset enable signal global_SR_EN2 346. This timing diagram shows that delay faults in functional logic can be tested with a double-capture approach, in accordance with the present invention. Note that delay faults can also be tested with a single-capture or last-shift-launch approach, in accordance with the present invention.

FIG. 5A shows an example set [[500]] of RTL (register-transfer level) Verilog codes before and after a sequentially-gated reset violation and a combinationally-gated reset violation are repaired, in accordance with the present invention.

Please replace the first paragraph on page 44 with the following amended paragraph:

FIG. 5C shows the gate-level circuit model 520 corresponding to the original RTL (register-transfer level) code shown in FIG. 5A. D flip-flops DFF2 522 (g1 output 533) and DFF3 523 (g2 output 532) are reset by asynchronous signals s_rst 531 and c_rst 532, respectively. Since the value of s_rst 531 is determined by an AND gate 524 with the output z 530 of the D flip-flop DFF1 521 as one of its inputs, this is a sequentially-gated reset violation. Since the value of c_rst 532 is determined by an AND gate 525 with only primary inputs rst 526 and x 527 as its inputs, this is a combinationally-gated reset violation.

On page 45, replace the paragraph beginning at line 13 with the following amended paragraph:

FIG. 5E shows the gate-level circuit model 560 corresponding to the original RTL (register-transfer level) code shown in FIG. 5B. D flip-flops DFF2 562 (having x input 564) and DFF3 563 (having a q2 output 570) are reset by asynchronous signals g_rst 567 and d_rst 568, respectively. Since the reset signal g_rst 567 of DFF2 562 comes directly from the D flip-flop DFF1 561 (having x input 564), this is a generated reset violation. Since the reset signal d_rst 568 of DFF3 563 is tied to VCC (logic value 1), this is a destructive reset violation.